ABSTRACT OF THE DISCLOSURE

A PWM signal generating circuit outputs a stable PWM signal for increasing and deceasing a duty ratio at a predetermined rate within a predetermined period without requiring an improvement of a process capacity of a CPU as compared to a conventional PWM signal generating circuit. The PWM signal generating circuit consists of a plurality of circuit elements each of which outputs a digital signal. A first counter circuit periodically changes a PWM signal output therefrom into an active state. A second counter circuit changes the PWM signal, which has been changed into the active state by the first counter circuit, into an inactive state within each cycle. The second counter circuit increases and decreases an active-to-inactive time period from a time when the PWM signal is changed into the active state to a time when the PWM signal is changed into the inactive state.